REMARKS

The Examiner is thanked for the indication that claims 8-13, 19, 20, 30, and 31 are allowable if rewritten in independent form.

Claims 1-33 are pending in the instant application. Claims 1-7, 14-18, 21-29, and 32 presently stand rejected. Claims 1, 2, 4, 5, 7-14, 19, 22, and 30 are amended herein. Claim 11 is amended herein to stand as an independent claim. Claim 33 is newly presented. Entry of this amendment and reconsideration of the pending claims are respectfully requested.

Claim Objections

Claim 2 stands objected to as including redundant claim limitations. Applicants respectfully disagree. Claim 2 narrows claim 1 in a number of ways. First, claim 2 states that the first circuit comprises an enable circuit. Second, claim 2 states that the enable circuit "further" includes an enable input as well as the elements already recited as part of the "first circuit" namely "the circuit input" and "the circuit output." Third, claim 2 states that the enable input of the first circuit (renamed an enable circuit by claim 2) enables the delay circuit. Accordingly, Applicants respectfully disagree that claim 2 is redundant, but rather adds at least three distinguishing features.

Claim Rejections – 35 U.S.C. § 112

Claim 21 stands rejected under 112, second paragraph, as omitting essential structural connections between the following elements: one of hardware behavioral code, register transfer level code, a netlist, a circuit layout, a clock enable circuit, a falling edge delay circuit, and a rising edge delay circuit.

Claim 21 has been amended to recite, "wherein the description comprises one of a hardware behavioral code, register transfer level code, a netlist, **or** a circuit layout." As described in paragraph [0050] of the specification, hardware behavioral code, register transfer level code, a netlist, **or** a circuit layout each represent different levels of abstraction to describe an integrated circuit. Accordingly, claim 21 simply states that "the description" (introduced in the preamble of claim 14) of the integrated circuit comprises one of the following levels of abstraction: hardware behavioral code, register

transfer level code, a netlist, **or** a circuit layout. It does not make any sense to talk about structural connections between the type of the description (i.e., hardware behavioral code, register transfer level code, a netlist, a circuit layout) and the elements described by the description.

Examiners "should not reject claims or insist on their own preferences if other modes of expression selected by applicants satisfy the statutory requirement." M.P.E.P. § 2173.02. "Definiteness of claim language must be analyzed, not in a vacuum, but in light of: (A) ***The content of the particular application disclosure***; (B) The teachings of the prior art; and (C) The claim interpretation that would be given by one possessing the ordinary level of skill in the pertinent art at the time the invention was made" (Emphasis added). M.P.E.P. § 2173.02. Applicants respectfully submit that one of ordinary skill in the art would understand the meaning of claim 21.

Claim 28 stands rejected under § 112, second paragraph, as omitting essential structural cooperative relationships between a microprocessor, a clock distribution network, and a clock delay circuit. Claim 28 redefines the integrated circuit recited in the preamble of claim 22 as a microprocessor, therefore, the elements in the body of claim 22 are subcomponents of the microprocessor. Again, it makes no sense to talk in terms of structural cooperative relationships between the integrated circuit (redefined in claim 28 as a microprocessor) and the subcomponents of the integrated circuit. The subcomponents collectively make up at least a portion of the microprocessor.

It is noteworthy that claim 28 recites, "the integrated circuit **comprises** a microprocessor" as opposed to "the integrated circuit **further comprising** a microprocessor." Again, applicants believe one of ordinary skill in the art would understand the meaning of claim 28.

Claim Rejections – 35 U.S.C. § 102

Claims 1 and 3-7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Tang (US 6,859,082).

A claim is anticipated only if each and every element of the claim is found in a single reference. M.P.E.P § 2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628 (Fed. Cir. 1987)). "The identical invention must be shown in

as complete detail as is contained in the claim." M.P.E.P. § 2131 (citing *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226 (Fed. Cir. 1989)).

Independent claim 1 now recites, in pertinent part,

> a first circuit including:
> a circuit input to receive a reference signal;
> a circuit output to output a delayed signal being a delayed response to the reference signal;
> a logic circuit including a logic input and a logic output, the logic input coupled to the circuit input to generate an inversion of the reference signal at the logic output;
> a pull up path coupled to the logic output; and
> a pull down path coupled to the logic output;
> a falling edge delay circuit **coupled to the pull up path** to control delay of a falling edge of the reference signal; and
> a rising edge delay circuit **coupled to the pull down path** to control delay of a rising edge of the reference signal.

Applicants respectfully submit that Tang fails to disclose the recited logic circuit, pull up path, pull down path, falling edge delay circuit, and rising edge delay circuit configuration.

To be sure, the Examiner cites FIGs. 3, 4, and 9 of Tang as the basis for rejecting claim 1. However, amended independent claim 1 now recites a pull up path and a pull down path coupled to the output of a logic circuit with the pull up path coupled to a falling edge delay circuit and the pull down path coupled to a rising edge delay circuit. Clearly, FIGs 3 and 4 fail to disclose this configuration. In particularly, the Examiner cites DCSR 340 and DCSK 350 illustrated in FIG. 3 of Tang as corresponding to Applicants claimed falling edge delay circuit and rising edge delay circuit, respectively. However, DCSR 340 and DCSK 350 clearly do not couple to a logic output of a logic circuit. In fact, DCSR 340 and DCSK 350 don't even couple to the same circuit node, much less to a circuit node which is a logic circuit output.

Consequently, Tong fails to disclose each and every element of claim 1, as required under M.P.E.P. § 2131. Accordingly, Applicants request that the instant §102 rejection of claim 1 be withdrawn.

Claim Rejections – 35 U.S.C. § 103

Claims 2 and 14-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang in view of Lee (US 6,462,597). Claims 22-27, 29, and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tang in view of Kliza et al. (US 5,852,640), in further view of admitted prior art.

"To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. All words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03.

Amended independent claim 14 now recites, in pertinent part,

> a circuit output to output a delayed clock signal being a delayed response to the reference clock signal;
>
> a **NAND logic circuit** having a first NAND input coupled to receive the reference clock signal, a second NAND input coupled to the enable input, and a NAND output; and
>
> an **inverter circuit coupling the NAND output to the circuit output**;

Applicants respectfully submit that the combination of Tang and Lee fails to teach or suggest a NAND logic circuit and an inverter circuit coupled within a clock enable circuit as recited in claim 14.

Consequently, the combination of Tang and Lee fails to teach or suggest all elements of claim 14, as required under M.P.E.P. § 2143.03. Independent claim 22 now includes similar nonobvious elements as independent claim 14. Accordingly, Applicants request that the instant §103(a) rejections of claims 14 and 22 be withdrawn.

The dependent claims are patentable over the prior art of record for at least the same reasons as discussed above in connection with their respective independent claims, in addition to adding further limitations of their own. Accordingly, Applicants respectfully request that the instant § 102 and § 103 rejections for the dependent claims be withdrawn.

Amended Independent Claim 11

Claim 11 has been amended into independent form. Claim 11 recites an "inverting enable circuit ... to output a delayed signal being a delayed inversion of the

reference signal..." Applicants respectfully submit that the prior art of record fails to disclose, teach, or fairly suggest this claim element.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants believe the applicable rejections have been overcome and all claims remaining in the application are presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative at (206) 292-8600 if the Examiner believes that an interview might be useful for any reason.

CHARGE DEPOSIT ACCOUNT

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a). Any fees required therefore are hereby authorized to be charged to Deposit Account No. 02-2666. Please credit any overpayment to the same deposit account.

Respectfully submitted,

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